

Appl. No. 10/687,183
Amdt. dated April 21, 2006
Response to Office Action of 01/24/2006

Attorney Docket No.: TS03-120
N1085-90157

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1 1. (Withdrawn) A method of forming a copper interconnect on a substrate,
2 comprising:

3 (a) providing a substrate with a dielectric layer formed thereon;

4 (b) forming a pattern comprised of at least one opening having a low pattern
5 density in a first region and at least one opening having a high pattern density in a
6 second region in said dielectric layer, each of said openings having sidewalls and a
7 bottom;

8 (c) depositing a conformal diffusion barrier layer on said dielectric layer and
9 on the sidewalls and bottom of said openings and depositing a first copper layer on the
10 diffusion barrier layer that fills said openings;

11 (d) performing a first planarization process that removes the first copper layer
12 and diffusion barrier layer above the dielectric layer and forms a dished upper surface
13 on the planarized first copper layer in said openings, said planarized first copper layer
14 has a first thickness;

15 (e) forming a second copper layer on said planarized first copper layer by a
16 selective deposition process, said second copper layer extends to a level above said
17 dielectric layer;

18 (f) annealing said planarized first copper layer and said second copper layer;
19 and

20 (g) performing a second planarization process so that the second copper
21 layer becomes coplanar with said dielectric layer and wherein the planarized and
22 annealed second copper layer has a second thickness and a grain density G_{D2} and, the
23 planarized and annealed first copper layer has a grain density G_{D1} .

1 2. (Withdrawn) The method of claim 1 wherein said dielectric layer is comprised of
2 SiO_2 , borophosphosilicate glass, or a low k dielectric material that is fluorine doped

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3 SiO₂, carbon doped SiO₂, a poly(arylether), a polysilsesquioxane, benzocyclobutene, or
4 a fluorinated polyimide and has a thickness of about 3000 to 7000 Angstroms.

1 3. (Withdrawn) The method of claim 1 wherein said substrate is comprised of an
2 upper etch stop layer with a thickness of about 100 to 2000 Angstroms and the
3 openings formed in said dielectric layer extend through said etch stop layer.

1 4. (Withdrawn) The method of claim 1 wherein said diffusion barrier layer is Ta,
2 TaN, Ti, TiN, W, WN, or TaSiN and has a thickness between about 10 and 1000
3 Angstroms.

1 5. (Withdrawn) The method of claim 1 wherein an opening is comprised of a via,
2 trench, or a trench formed above a via and wherein the width of said openings ranges
3 from about 0.1 microns to over 10 microns.

1 6. (Withdrawn) The method of claim 1 wherein said openings formed in said first
2 region and said openings formed in said second region have equivalent widths.

1 7. (Withdrawn) The method of claim 1 wherein the process of depositing said first
2 copper layer comprises a first step of forming a copper seed layer on said diffusion
3 barrier layer by a physical vapor deposition (PVD) or ionized metal plasma (IMP)
4 process and a second step of depositing copper to fill said opening by a PVD,
5 electroplating, or an electroless plating method.

1 8. (Withdrawn) The method of claim 1 wherein said first planarization process is a
2 chemical mechanical polish (CMP) step.

1 9. (Withdrawn) The method of claim 1 wherein said second copper layer is formed
2 by a selective electroless plating or electrochemical deposition process.

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1 10. (Withdrawn) The method of claim 9 wherein said electroless plating process is
2 comprised of treating said substrate with an aqueous solution having a pH of about 8 to
3 13 and a temperature of about 67°C to 73°C and comprised of the following: $\text{CuSO}_4 \cdot 5\text{H}_2\text{O}$
4 with a concentration of 10 grams per liter (g/L), a 37% formaldehyde solution in water at
5 a concentration of 15 ml/L, EDTA with a concentration of 28 g/L, tetramethylammonium
6 hydroxide (TMAH) with a concentration of 125 g/l, KOH with a concentration of 18.5 g/L,
7 and 2,2-bipyridine at a concentration of 1.5 g/L.

1 11. (Withdrawn) The method of claim 1 wherein said annealing process is
2 performed by heating said substrate in an oven at a temperature of about 150°C to
3 300°C in an inert atmosphere comprised of N_2 , Ar, or H_2 for a period of about 10
4 seconds to 5 minutes.

1 12. (Withdrawn) The method of claim 1 wherein said second planarization process
2 is a CMP buffing step involving a down force of about 2 to 4 psi and a slurry comprised
3 of SiO_2 , H_2O , and a basic component which is NaOH, KOH or NH_4OH .

1 13. (Withdrawn) The method of claim 1 wherein the planarized first copper layer has
2 a thickness equal to or greater than the thickness of the planarized second copper
3 layer.

1 14. (Withdrawn) The method of claim 1 wherein G_{D1} is greater than or equal to G_{D2} .

1 15. (Withdrawn) The method of claim 1 wherein the sheet resistance (R_s) for a
2 copper interconnect comprised of the planarized and annealed first copper layer and the
3 planarized and annealed second copper layer is nearly independent of the pattern
4 density of the region in which said copper interconnect is formed.

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1 16. (Withdrawn) The method of claim 1 wherein the Rs for a copper interconnect
2 comprised of the planarized and annealed first copper layer and the planarized and
3 annealed second copper layer is nearly independent of the width of the opening in
4 which said copper interconnect is formed.

1 17. (Withdrawn) A method of forming a copper interconnect on a substrate,
2 comprising:

3 (a) providing a substrate with a dielectric layer formed thereon;

4 (b) forming at least one opening having a first width in a first region in said
5 dielectric layer and at least one opening having a second width that is unequal to said
6 first width in a second region in said dielectric layer, each of said openings having
7 sidewalls and a bottom;

8 (c) depositing a conformal diffusion barrier layer on said dielectric layer and
9 on the sidewalls and bottoms of said openings and depositing a first copper layer on the
10 diffusion barrier layer that fills said openings;

11 (d) performing a first planarization process that removes the first copper layer
12 and diffusion barrier layer above the dielectric layer and forms a dished upper surface
13 on the planarized first copper layer in said openings, said planarized first copper layer
14 has a first thickness;

15 (e) forming a second copper layer on the planarized first copper layer by a
16 selective deposition process, said second copper layer extends to a level above said
17 dielectric layer;

18 (f) annealing the planarized first copper layer and said second copper layer;
19 and

20 (g) performing a second planarization process so that the second copper
21 layer becomes coplanar with said dielectric layer and wherein the planarized and
22 annealed second copper layer has a second thickness and a grain density G_{D2} and the
23 planarized and annealed first copper layer has a grain density G_{D1} .

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1 18. (Withdrawn) The method of claim 17 wherein said dielectric layer is comprised
2 of SiO₂, borophosphosilicate glass, or a low k dielectric material that is fluorine doped
3 SiO₂, carbon doped SiO₂, a poly(arylether), a polysilsesquioxane, benzocyclobutene, or
4 a fluorinated polyimide and has a thickness of about 3000 to 7000 Angstroms.

1 19. (Withdrawn) The method of claim 17 wherein said substrate is further comprised
2 of an upper etch stop layer with a thickness of about 100 to 2000 Angstroms and the
3 openings formed in said dielectric layer extend through said etch stop layer.

1 20. (Withdrawn) The method of claim 17 wherein said diffusion barrier layer is Ta,
2 TaN, Ti, TiN, W, WN, or TaSiN and has a thickness between about 10 and 1000
3 Angstroms.

1 21. (Withdrawn) The method of claim 17 wherein the width of said openings ranges
2 from about 0.1 microns to over 10 microns.

1 22. (Withdrawn) The method of claim 17 wherein the process of depositing said first
2 copper layer comprises a first step of forming a copper seed layer on said diffusion
3 barrier layer by a PVD or IMP process and a second step of depositing copper to fill
4 said opening by a PVD, electroplating, or electroless plating method.

1 23. (Withdrawn) The method of claim 17 wherein said first planarization process is a
2 chemical mechanical polish (CMP) step.

1 24. (Withdrawn) The method of claim 17 wherein said second copper layer is
2 formed by a selective electroless plating or electrochemical deposition process.

1 25. (Withdrawn) The method of claim 24 wherein said electroless plating process is
2 comprised of treating said substrate with an aqueous solution having a pH of about 8 to
3 13 and a temperature of about 67°C to 73°C and comprised of the following:

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4 CuSO₄5H₂O with a concentration of 10grams (g)/liter (L); a 37% formaldehyde solution
5 in water with a concentration of 15 ml/L; EDTA with a concentration of 28 g/L;
6 tetramethylammonium hydroxide (TMAH) at a concentration of 125 g/L; KOH with a
7 concentration of 18.5 g/L; and 2,2-bipyridine with a concentration of 1.5 g/L.

1 26. (Withdrawn) The method of claim 17 wherein said annealing process is
2 performed by heating said substrate in an oven at a temperature of about 150°C to
3 300°C in an inert atmosphere comprised of N₂, Ar, or H₂ for a period of about 10
4 seconds to 5 minutes.

1 27. (Withdrawn) The method of claim 17 wherein said second planarization process
2 is a CMP buffing step involving a down force of about 2 to 4 psi and a slurry comprised
3 of SiO₂, H₂O, and a basic component which is NaOH, KOH or NH₄OH.

1 28. (Withdrawn) The method of claim 17 wherein the planarized first copper layer
2 has a thickness equal to or greater than the thickness of the planarized second copper
3 layer.

1 29. (Withdrawn) The method of claim 17 wherein G_{D1} is greater than or equal to G_{D2}.

1 30. (Withdrawn) The method of claim 17 wherein the R_s for a copper interconnect
2 formed in an opening in said first region is nearly equivalent to the R_s for a copper
3 interconnect formed in an opening in said second region.

1 31. (Withdrawn) The method of claim 17 wherein the sheet resistance for a copper
2 interconnect comprised of the planarized and annealed first copper layer and the
3 planarized and annealed second copper layer is nearly independent of the pattern
4 density of the region in which said copper interconnect is formed.

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1 32. (Withdrawn) The method of claim 17 further comprised of forming a plurality of
2 openings in a plurality of regions in said dielectric layer, said openings having a plurality
3 of widths.

1 33. (Withdrawn) The method of claim 32 wherein the copper interconnect comprised
2 of the planarized and annealed first copper layer and the planarized and annealed
3 second copper layer has a Rs that is nearly independent of the width of the opening in
4 which said copper interconnect is formed.

1 34. (Currently Amended) A copper interconnect structure in a semiconductor device,
2 comprising:

3 (a) a first copper layer having first substantially vertical sidewalls, a planar
4 bottom, and a concave top surface formed in an opening in a dielectric layer on a
5 substrate, said first copper layer having a first thickness and a grain density G_{D1} , said
6 first substantially vertical sidewalls disposed along sides of said opening; and

7 (b) a second copper layer disposed in said opening and having second
8 substantially vertical sidewalls disposed along said sides of said opening, a substantially
9 planar top surface that is about coplanar with the top of said dielectric layer, and a
10 convex bottom surface that forms an interface with said concave top surface of said first
11 copper layer, said second copper layer having a second thickness and a grain density
12 G_{D2} .

1 35. (Original) The copper interconnect of claim 34 wherein said substrate is
2 further comprised of an upper etch stop layer and the opening extends through said
3 etch stop layer.

1 36. (Original) The copper interconnect of claim 34 wherein said dielectric layer is
2 comprised of SiO_2 , borophosphosilicate glass, or a low k dielectric material that is

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3 fluorine doped SiO₂, carbon doped SiO₂, a poly(arylether), a polysilsesquioxane,
4 benzocyclobutene, or a fluorinated polyimide.

1 37. (Original) The copper interconnect structure of claim 34 wherein the
2 combined thickness of said first copper layer and said second copper layer is from
3 about 3000 to 7000 Angstroms.

1 38. (Currently Amended) The copper interconnect structure of claim 34 further
2 comprised of a conformal diffusion barrier layer formed in said opening along the first
3 substantially vertical sidewalls and bottom of said first copper layer and along the
4 second substantially vertical sidewalls of said second copper layer.

1 39. (Original) The copper interconnect structure of claim 34 wherein the width of
2 said first copper layer and the width of said second copper layer have a range from
3 about 0.1 microns to over 10 microns.

1 40. (Original) The copper interconnect structure of claim 34 wherein said copper
2 interconnect has a sheet resistance that is nearly independent of the width of said first
3 copper layer and the width of said second copper layer.

1 41. (Original) The copper interconnect structure of claim 34 wherein said opening
2 is part of a pattern that includes a plurality of other openings having a pattern density
3 and said copper interconnect has a sheet resistance (Rs) that is nearly independent of
4 said pattern density.

1 42. (Original) The copper interconnect structure of claim 34 wherein the first
2 thickness of said first copper layer is equal to or greater than the second thickness of
3 said second copper layer.

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1 43. (Original) The copper interconnect structure of claim 34 wherein G_{D1} is
2 greater than or equal to G_{D2} .

1 44. (Original) The copper interconnect structure of claim 34 wherein said
2 substrate is comprised of a metal layer and said first copper layer of said copper
3 interconnect is formed above said metal layer and forms an electrical contact to said
4 metal layer.

1 45. (Currently Amended) A copper interconnect formed in an opening comprised of
2 a trench formed above a via in a dielectric layer on a substrate, said trench having
3 trench sidewalls, a bottom, and a width that is larger than the width of said via and said
4 via having via sidewalls and a bottom, comprising:

5 (a) a first copper layer that fills said via and extends into said trench, said first
6 copper layer having lower substantially vertical sidewalls and a planar bottom in said via
7 and first substantially vertical sidewalls that are disposed along said trench sidewalls
8 and a planar bottom in said trench, a concave top surface formed within the trench, a
9 first thickness, and a grain density G_{D1} ; and

10 (b) a second copper layer formed within the trench portion of said opening
11 and having second substantially vertical sidewalls that are disposed along said trench
12 sidewalls, a substantially planar top surface that is about coplanar with the top of said
13 dielectric layer and the top of the trench, and a convex bottom surface that forms an
14 interface with the concave top surface of said first copper layer, said second copper
15 layer having a second thickness and a grain density G_{D2} .

1 46. (Original) The copper interconnect of claim 45 wherein said substrate is
2 further comprised of an upper etch stop layer and the via extends through said etch stop
3 layer.

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1 47. (Original) The copper interconnect of claim 45 wherein the combined
2 thickness of said first copper layer and said second copper layer is from about 3000 to
3 7000 Angstroms.

1 48. (Currently Amended) The copper interconnect of claim 45 further comprised
2 of a conformal diffusion barrier layer formed along the lower substantially vertical
3 sidewalls and first substantially vertical sidewalls of the first copper layer and the
4 second substantially vertical sidewalls of the second copper layer and along the bottom
5 of the first copper layer in the trench and via.

1 49. (Original) The copper interconnect of claim 45 wherein said copper
2 interconnect has a sheet resistance that is nearly independent of the width of the trench.

1 50. (Original) The copper interconnect of claim 45 wherein said opening is part of
2 a pattern that includes a plurality of other openings having a pattern density and said
3 copper interconnect has a sheet resistance (R_s) that is nearly independent of said
4 pattern density.

1 51. (Original) The copper interconnect of claim 45 wherein the first thickness of
2 said first copper layer is equal to or greater than the second thickness of said second
3 copper layer.

1 52. (Original) The copper interconnect structure of claim 45 wherein G_{D1} is
2 greater than or equal to G_{D2} .